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Real-time implementation of an efficient Golay correlator (EGC) applied to ultrasonic sensorial systems

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Abstract

Multi-mode techniques reduce scanning times in ultrasonic systems, as they allow transducers in a sensor to simultaneously emit and receive without interference. In order to implement these techniques, it is necessary to encode each transducer's emission. The use of orthogonal pairs of Golay sequences associated with different emitters avoids crosstalk among them. However, these sequences imply an increase in the computational complexity required in the receiver. This paper presents the practical implementation of a system, with two emitters and four receivers, using a low-cost hardware architecture based on a FPGA. The ultrasonic signal processing is performed in real time.

Keywords: Ultrasonic system; Multi-emission; Golay sequences; FPGA

1. Introduction

One of the drawbacks implicit in a sensorial system based on ultrasonic transducers is the length of involved scanning time. Numerous proposals have been made to improve this aspect. Among them, some of the most noteworthy are those that attempt to reduce these times by enabling various transducers to emit simultaneously, without interfering with another one, and designing a receiver that is able to discern the source of the emission [3]. If this is to be achieved by encoding the source, a different sequence has to be available for each emitter, which requires a high degree of auto-correlation (ideally a Kroenecker delta), and a zero cross-correlation with the rest of the sequences existing in the system (orthogonal sequences).

Pairs of complementary Golay sequences [1,2] present these characteristics, what means that they are ideal for this purpose. However, their use causes a considerable increase in computations, especially in blocks in the reception stage of each transducer used to detect the various emissions produced in the system. These detection processes for the signal received by each transducer need to be carried out in real time, so that the times-of-flight obtained from the detected echoes are available for higher level tasks (obstacle classification, map generation, etc.) [8]. This computational increase, together with the restrictions of real-time operation, implies greater hardware complexity, minimizing one of the main advantages of this type of sensorial system: their simplicity and low cost.

In this paper, a sensor consisting of four ultrasonic receivers (E/R1, R2, R3 and E/R4) [7,8] has been used; only two also function as emitters—E/R1 and E/R4—(each of them is associated with a pair of orthogonal complementary Golay sequences). In Fig. 1 it is possible to observe the geometric distribution of the transducers; the emitters/receivers are placed at the edges of the structure, whilst the two central transducers work solely as receivers. For a reflector P, it is possible to obtain four times-of-flight for a single emission. These values are later used to compute the distance from the reflector to each of the transducers (r_1, r_2, r_3 and r_4), as well as to determine the reception angles (θ_1 and θ_4).

The following sections show the implementation of the aforementioned system on an architecture based on a low-cost FPGA device and an external memory bank, needed to store the intermediate results of the algorithm.

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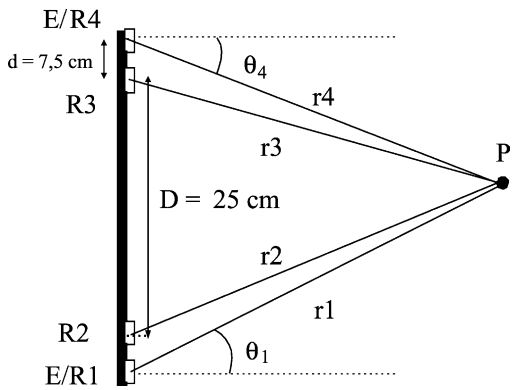

Fig. 1. Geometric distribution of the ultrasonic transducers in a sensor.

2. Proposed algorithm

The possibility of using pairs of orthogonal complementary Golay sequences to determine the times-of-flight of the ultrasonic emissions has been demonstrated in previous papers [1]. These pairs are composed of two sequences, A and B, of length N and values $\{-1,+1\}$, whose auto-correlation, and later addition, provides an output signal in accordance with expression (1)

$$C_{AA}[n] + C_{BB}[n] = \begin{cases} 2N, & n = 0 \\ 0, & n \neq 0 \end{cases} \quad (1)$$

where $C_{AA}[n]$ and $C_{BB}[n]$ are the auto-correlations of each sequence of the pair, and N is the number of bits or length of the sequences.

In order to make use of these sequences, an ultrasonic signal processing algorithm has been developed. This is described below for a generic transducer functioning as either an emitter or a receiver. In the case of a transducer functioning only as a receiver, it is necessary to eliminate the modules used in the emission stage, leaving everything else unchanged.

The block diagram in Fig. 2 shows the different modules that make up the basic system -for a single transducer i. An emission stage is included that enables the pair of Golay sequences associated with the mentioned transducer i to be emitted. This stage consists firstly of QPSK modulation of the pair of complementary Golay sequences. This modulation is necessary because the used ultrasonic signals transducer [5] has a bandwidth that is restricted to around 50 kHz, not being possible to emit the pair of sequences directly on the baseband. Having first passed through a signal conditioning stage, the signal obtained in the modulation will be used to excite the transducer.

With regard to the reception stage, in a system based on two simultaneous emitters, each receiver can capture echoes from two different sources (itself and another transducer). This implies that detection should involve the search for the associated pairs of sequences. The acquired signal, after a conditioning and analogue-digital conversion stage, is then processed by the reception stage using a sampling frequency of 400 kHz (a frequency high enough to enable the emitted signal to be recovered, modulated using a carrier frequency of 50 kHz). The first step consists of carrying out demodulation in order to obtain the components i (in phase) and Q (in quadrature) typical of the used modulation. Taking the components i and Q, the search for the complementary A and B sequences is initiated, using two stages based on correlation processes. Finally, the result of these is calculated and processed to detect local maximums, what determines the presence of possible ultrasonic echoes in the captured signal. It should be considered that it is necessary to search for two pairs of different complementary Golay sequences, corresponding to the two transducers/emitters that make up the overall system.

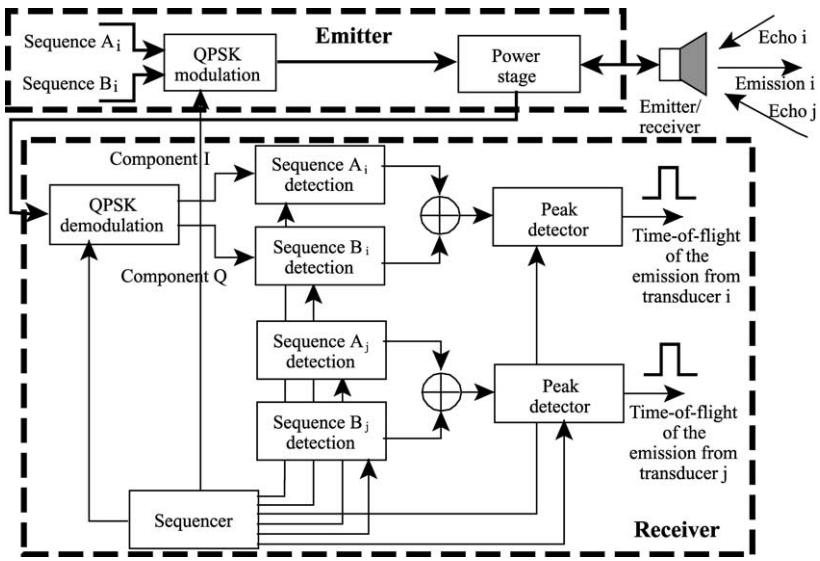

Fig. 2. General block diagram of the system associated with an ultrasonic emitter/receiver.

Table 1
Symbols associated with the emission of each dibit of the pair of complementary sequences A and B

Dibit	Dibit symbol	Phase
00	$S_{00} = [-1\ -1\ -1\ -1\ +1\ +1\ +1\ +1\ -1\ -1\ -1\ -1\ +1\ +1\ +1\ +1]$	0
10	$S_{10} = [+1\ +1\ -1\ -1\ -1\ -1\ +1\ +1\ +1\ +1\ -1\ -1\ -1\ -1\ +1\ +1]$	$\pi/2$
11	$S_{11} = [+1\ +1\ +1\ +1\ -1\ -1\ -1\ -1\ +1\ +1\ +1\ +1\ -1\ -1\ -1\ -1]$	π
01	$S_{01} = [-1\ -1\ +1\ +1\ +1\ +1\ -1\ -1\ +1\ +1\ -1\ -1\ +1\ +1\ -1\ -1]$	$3\pi/2$

Finally, a synchronisation module (in Fig. 2 it is called a sequencer) is used to control the proper operation of the various modules and stages that constitute the sonar module for two emitters.

The following sections describe these modules in detail, indicating the algorithmics associated with them, as well as showing the proposed block diagrams that determine their subsequent physical implementation on a FPGA device.

2.1. Emitter module

In order to be able to emit the pair of complementary Golay sequences at the transducer's maximum response frequency [5], a digital variant of QPSK modulation has been performed. The system's emitter consists of a QPSK modulator, whose function is to encode the sequence A of the Golay pair on the component in phase i, while the component in quadrature Q is associated with sequence B. Thus, the obtained signal $e[n]$ is the input of the conditioning stage that excites the ultrasonic transducer.

Each pair of bits, one from the sequence $A_i[n]$ and the other from the sequence $B_i[n]$, both associated with transducer i, form a dibit that corresponds to a point in the constellation of the used QPSK modulation

$$A_i[n] = [a_{i0}, a_{i1}, \ldots, a_{i(N-2)}, a_{i(N-1)}] \quad (2)$$

$$B_i[n] = [b_{i0}, b_{i1}, \ldots, b_{i(N-2)}, b_{i(N-1)}]$$

Expression (3) shows the symbols $S_I[n]$ and $S_Q[n]$, used respectively for the component in phase $i$and for the component in quadrature Q. Two periods of a 50 kHz square signal have been chosen for each symbol. As this signal is later sampled at 400 kHz, a total of 16 samples exist in each symbol. The symbol associated with each dibit in the emission is obtained from the combination of these for each of the four possible existing dibits, (see Table 1).

$$S_I[n] = [1\ 1\ 0\ 0\ -1\ -1\ 0\ 0\ 1\ 1\ 0\ 0\ -1\ -1\ 0\ 0] \quad (3)$$

$$S_Q[n] = [0\ 0\ 1\ 1\ 0\ 0\ -1\ -1\ 0\ 0\ 1\ 1\ 0\ 0\ -1\ -1]$$

$$S_Q[n] = S_I[n-2]$$

By analysing the sequence or symbol that should be emitted for each dibit, it may be observed that to generate the symbol of the dibit XY the following sequence is complied (they are associated in two-figure groups).

$$S_{XY}[n] = [X\ X\ Y\ Y\ -X\ -X\ -Y\ -Y\ X\ X\ Y\ Y\ -X\ -X\ -Y\ -Y] \quad (4)$$

Thus, the symbol of each dibit can be generated from it, using appropriate multiplexing of the two bits, as well as using an OR-exclusive gate that enables a bit to be inverted at the desired moment (see Fig. 3). The pair of complementary Golay sequences is stored in both FIFO memories, having both a depth equal to the length N of the selected sequences.

Lengths of 32 bits ($N = 32$) will be used. The bits that form these sequences are gradually read in groups of two, at the rate established by a 200 kHz-frequency clock signal, so that the desired values are obtained in the signal $e_i[n]$, using a carrier frequency of 50 kHz.

2.2. Receiver module

Once the characteristics of the transducer working in emitter mode have been specified, this has to then switch to receiver mode to detect the times-of-flight of the possible echoes that may have been produced. The system has been designed for a sampling frequency of 400 kHz, greater than that used in emission modulation. Use of this frequency means that, if it is desirable to process each new acquired sample in real time, a time of 2.5 μs is available for the entire analysis associated with it.

During this period of 2.5 μs, as it may be observed in Fig. 2, the processing of a particular sample has to be divided into the following stages:

- *First correlation*. This is really a QPSK demodulation, in order to recover the components $I_i[n]$ (in phase) and $Q_i[n]$ (in quadrature) of the acquired signal $r_i[n]$ in a transducer i. To do so, it is necessary to take into account the symbol that was used in the corresponding modulation.

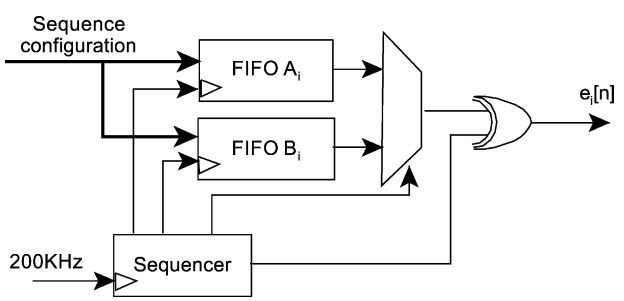

Fig. 3. Block diagram of the implementation of the ultrasonic transducer's emitter on an FPGA device.

- *Second correlation*. As the sequences A and B were assigned to the components i and Q, respectively in the emission process, it is necessary to search for them. A correlation of the components of the demodulation should be carried out using the two emitted Golay sequences. Bearing in mind that there are two emissions in the system, the search for the components i and Q should be duplicated for each emitted Golay pair. The results of these two correlations are added to obtain a final signal, in accordance with the properties of the Golay sequences described earlier. This signal is then analysed to detect the existing local maximums, and to validate them as received echoes.

2.2.1. First correlation

This is the first stage of the detection algorithm. The signal sampled at 400 kHz is correlated with the symbol $S_I[n]$ to demodulate and obtain the signal $I_i[n]$, as it is shown in expression (5). The process to obtain the component $Q_i[n]$ is analogous, being necessary to use the symbol $S_Q[n]$

$$I_i[n] = C_{rS_I}[n] = \sum_{k=0}^{15} r_i[k+n]S_Q[k+2] \tag{5}$$

$$Q_i[n] = C_{rS_Q}[n] = \sum_{k=0}^{15} r_i[k+n]S_Q[k]$$

where the signals $S_I[n]$ and $S_Q[n]$ were defined in expression (3), complying $S_Q[n] = S_I[n-2]$. This characteristic may be used to reduce the hardware required for this first correlation (Fig. 4) .

Thus, the demodulation stage of the received signal may be reduced to a single correlation. This correlation requires a certain depth of memory that allows the most recent samples acquired by the system to be constantly available. A simplified equation of the demodulation has been obtained using the equation in differences (6). It may be observed that the operation has been reduced to a set of additions and subtractions (without multiplications) of the last 16 samples acquired in the signal $r_i[n]$, depending on the bit of the corresponding symbol

$$\begin{aligned} Q_i[n] = {} & Q_i[n-1] - r_i[n-2] + r_i[n-4] + r_i[n-6] \\ & - r_i[n-8] - r_i[n-10] + r_i[n-12] \\ & + r_i[n-14] - r_i[n-16] \end{aligned} \tag{6}$$

In a low-cost FPGA, the internal implementation of the memory, needed to store the samples required in the process,

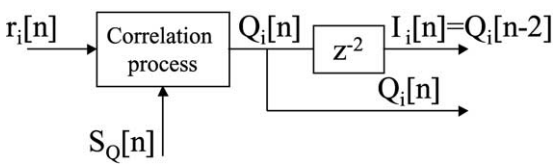

Fig. 4. Reduction of the implemented demodulation stage.

is an excessively costly procedure. Therefore, an external memory device has been used to handle all of the intermediate data required in the overall process. This external memory is arranged in a circular buffer with a depth of 15 positions, the number of samples necessary to carry out the demodulation.

The implementation of the demodulation process, which constitutes the first correlation, is shown in Fig. 5. The accumulator, that carries out the process, takes samples from a circular memory zone. Here, the most recent samples of the acquired signal $r_i[n]$ are stored, saving the results $Q_i[n]$ in the buffer that will later be used by the second correlation. Only the signal corresponding to the component Q (in quadrature) is obtained. Thus, the system and the hardware resources, needed to carry out the demodulation and store its partial results, are simplified.

2.2.2. Second correlation

Once the component $Q_i[n]$ (in quadrature) is available, the next step is to perform detection of the possible sequences $A_x[n]$ and $B_x[n]$, where x represents a certain emitter index. These search processes are reflected in mathematical form as given below

$$\begin{aligned} s_{I_iA_x}[n] = C_{I_iA_x} &= \sum_{k=0}^{31} I_i[k\times 16+n]A_x[k] \\ &= \sum_{k=0}^{31} Q_i[k\times 16+n+2]A_x[k] \end{aligned} \tag{7}$$

$$s_{Q_iB_x}[n] = C_{Q_iBx} = \sum_{k=0}^{31} Q_i[k\times 16+n]B_x[k]$$

$$s_{ix}[n] = s_{I_iA_x}[n] + s_{Q_iB_x}[n]$$

Local maximums appear in signal $S_{ix}[n]$, coinciding with the detection of echoes caused by the emission of transducer x.

In order to implement the process, the results of the first correlation (demodulation) have been stored in an intermediate circular memory zone, which is accessed to obtain the components i and Q in the second correlation. Fig. 6 shows the general block diagram for this stage.

The hardware system has to access to the circular memory, in which the components of the demodulation are stored, equally spaced every 16 positions (decimation process). Data are successively accumulated, either in additions or subtractions, depending on the composition of the corresponding Golay sequence. As a result, the accumulators corresponding to the sequences $A_x[n]$ and $B_x[n]$ are controlled by the dibits of them.

However, this implementation of the Golay pair detector, although it is immediate and simple, is not the optimal solution. It has the drawback of having to carry out $2N$ accesses to the memory to obtain the earlier samples of the components $i$and Q. The use of a memory external to the FPGA device means that the system has to be designed to minimise the number of accesses to it. In this regard,

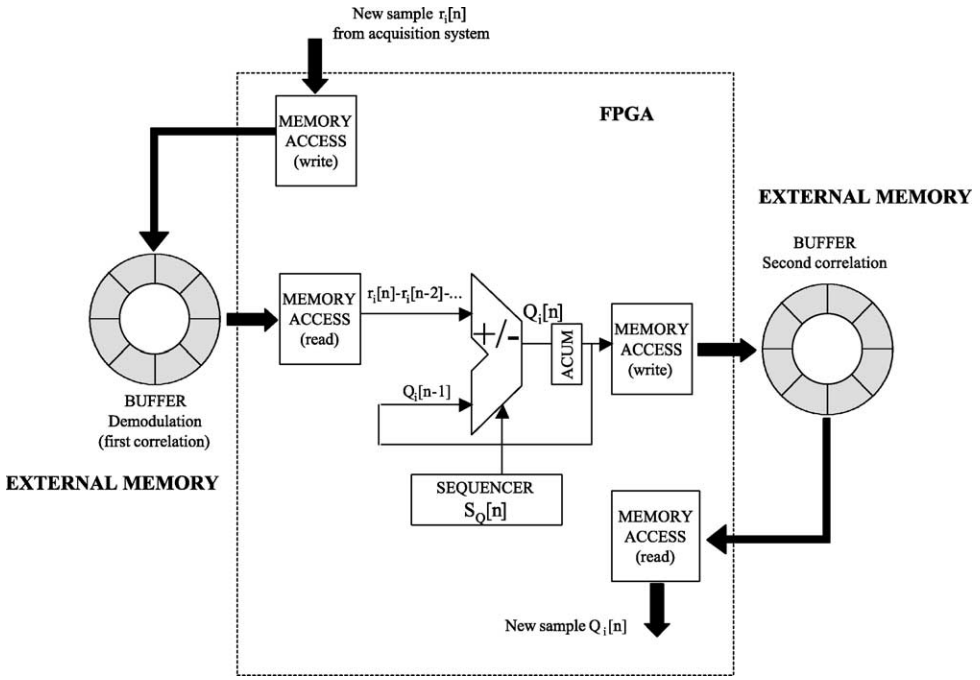

Fig. 5. Block diagram of the implementation used for the demodulation (first correlation).

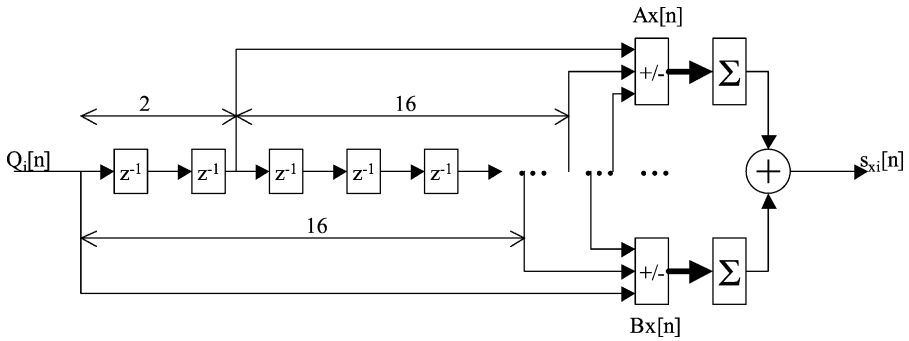

Fig. 6. General block diagram of the receiver's second correlation.

the EGC algorithm reduces the number of accesses, compared with the classic implementation of a correlator described here.

2.2.3. Efficient Golay correlator algorithm

Previous works [6] have led to the design and development of a new model of Golay sequence correlator, based on an inverse FIR filter structure. It is intended to take advantage of the characteristics of the Golay sequences, whose length is a power of 2. This type of sequences is generated from a seed $W = [w_1 w_2 \cdots w_s]$, so the final length N of the Golay pair is $N = 2^s$. The algorithm proposes a diagram like the one shown in Fig. 7, where it may be observed that it is possible to carry out the correlation of the signal $r_i[k]$ simultaneously with the pair $A[k]$ and $B[k]$. The two outputs from the filter correspond to the cross-correlation functions $C_{ra}[k]$ and $C_{rb}[k]$. The coefficients of this filter are the complex combinations of the bits used as the root to generate a pair of complementary Golay sequences. They may be simplified in accordance with expression (8), as they are real numbers

$$w_n \in \{+1, -1\}, \qquad w_n = w_n^* \tag{8}$$

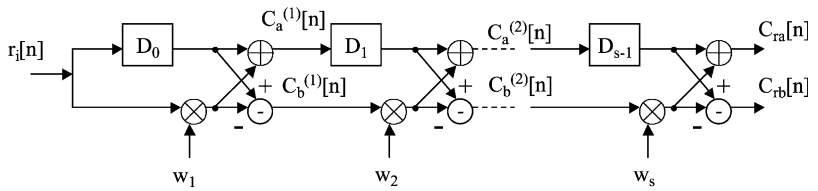

Fig. 7. Block diagram of the Efficient Golay Correlator (EGC).

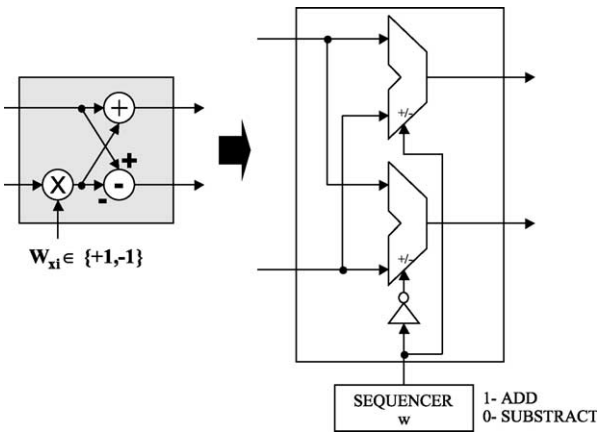

Fig. 8. Block diagram of the basic operation unit (OP).

Finally, the terms D_n mean delay blocks in memory positions; the depth of them grows geometrically with the advance of the filter, always in powers of 2.

This implementation supposes a total of $log_2 N$ multiplications, $2\ log_2 N$ additions, and $2\ log_2 N$ accesses to memory; meanwhile, the generic correlation method implies N multiplications, $N-1$ additions and N accesses to memory, being N the length of the Golay sequences.

The implementation of the mathematical model described in Fig. 7 includes the definition of an elemental operation module (OP), which is repeated regularly in the mentioned figure. Fig. 8 describes the OP unit, as well as its hardware implementation on a logic device. The performed operation, either addition or subtraction, is determined by the bit that corresponds to the seed of the searched Golay sequence.

The general block diagram is shown in Fig. 9; it consists of the OP units needed to detect a pair of complementary Golay sequences of length $N = 32$ bits, what implies a seed of $s = 5$ bits.

From this figure it may be deduced that it is possible to have two different types of implementation. On the one hand, exploiting the highest degree of parallelism in the application, it is possible to use as many basic OP units as needed for the spatial implementation of the algorithm. On the other, attempting to reduce the used hardware resources, it is possible to carry out a sequential implementation of the algorithm with a single OP unit. This unit is used sequentially to perform all of the required calculations. The following section shows the final temporal implementation carried out, based on the use of a single OP unit.

2.2.4. Hardware implementation of the receiver

The complete design is shown in Fig. 10. On the left-hand side, it is possible to observe the resources needed to implement demodulation; next, the detection of the pair of complementary Golay sequences is carried out using the EGC, based on a single basic OP unit. Finally, on the right-hand side, the memory manager may be observed. This controls and synchronises the accesses that the system has to make to the external memory to read or write the necessary partial results.

Based on the premise of real-time operation, the feasibility of this design should be assessed in terms of execution times. Bearing in mind that it is a synchronous digital system, with a clock frequency f_{CLK}, the following lines analyse the execution time of each of the phases of the reception process.

- Firstly, the system has to acquire and store a new sample in memory for subsequent processing. This operation needs a clock period T_{CLK}.
- Demodulation is mathematically formulated in expression (6), in which it may be observed that a total of eight accesses to external memory are necessary to obtain the required samples from $r_i[N]$. This involves an execution time, supposing one access per clock cycle, of $8T_{CLK}$.
- Finally, the greater complexity of the aforementioned design is based on controlling the accesses to memory during the second correlation, which is arranged in accordance with the diagram in Fig. 11. The sequence of accesses needed to detect two possible emissions, corresponding to both transducers, is shown. The process starts with the acquisition of a new sample $Q_i[n]$, from which the EGC algorithm is

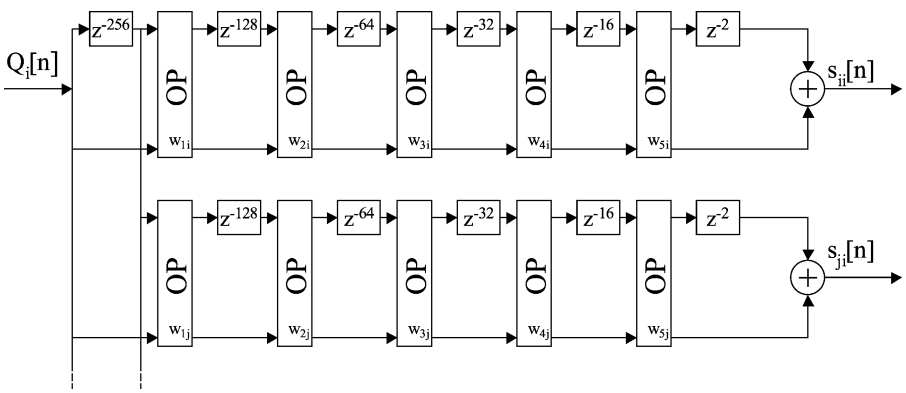

Fig. 9. Implementation of the Efficient Golay Correlator (EGC).

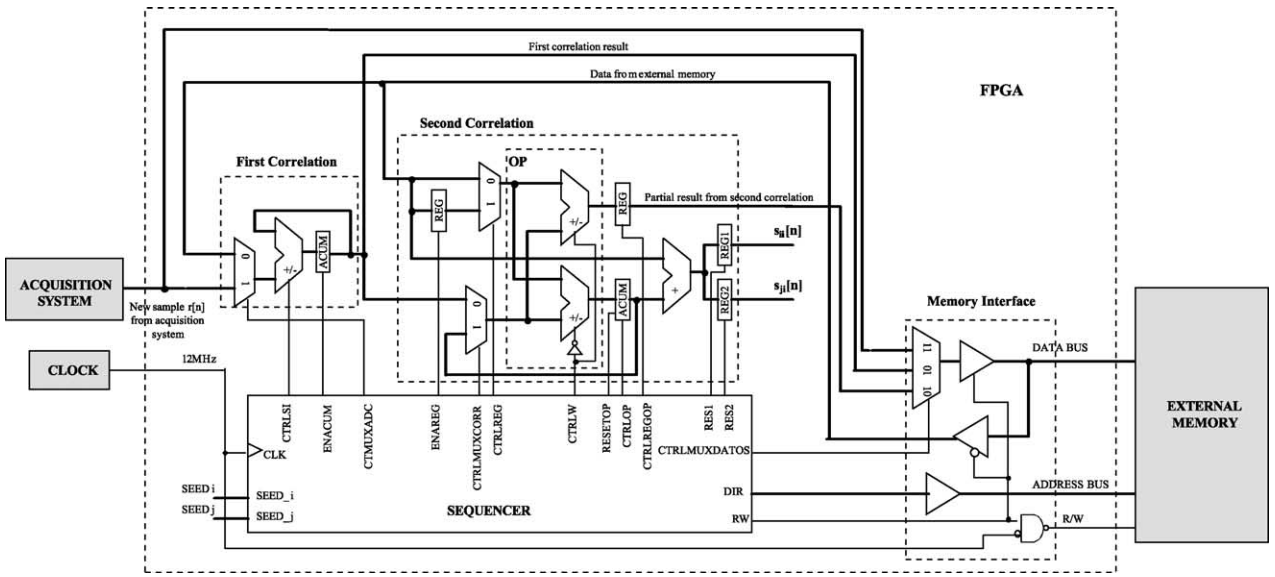

Fig. 10. Receiver implementation of an ultrasonic transducer used to detect two different emissions.

developed. This involves writing the partial results in the intermediate circular memory zones, so only the last 256 acquired samples may be used in the search for the two mentioned pairs of Golay sequences. The rest of the buffer, up to the 512 samples needed to implement the second correlation, should be duplicated, assigned one to each detection. Thus, the calculation requires an execution time of $22T_{CLK}$, for the case of two different emissions.

Overall, the system requires 30 clock cycles T_{CLK} to successfully complete the processing of each new sample; considering that a new sample is obtained every 2.5 μs, the minimum operating frequency of

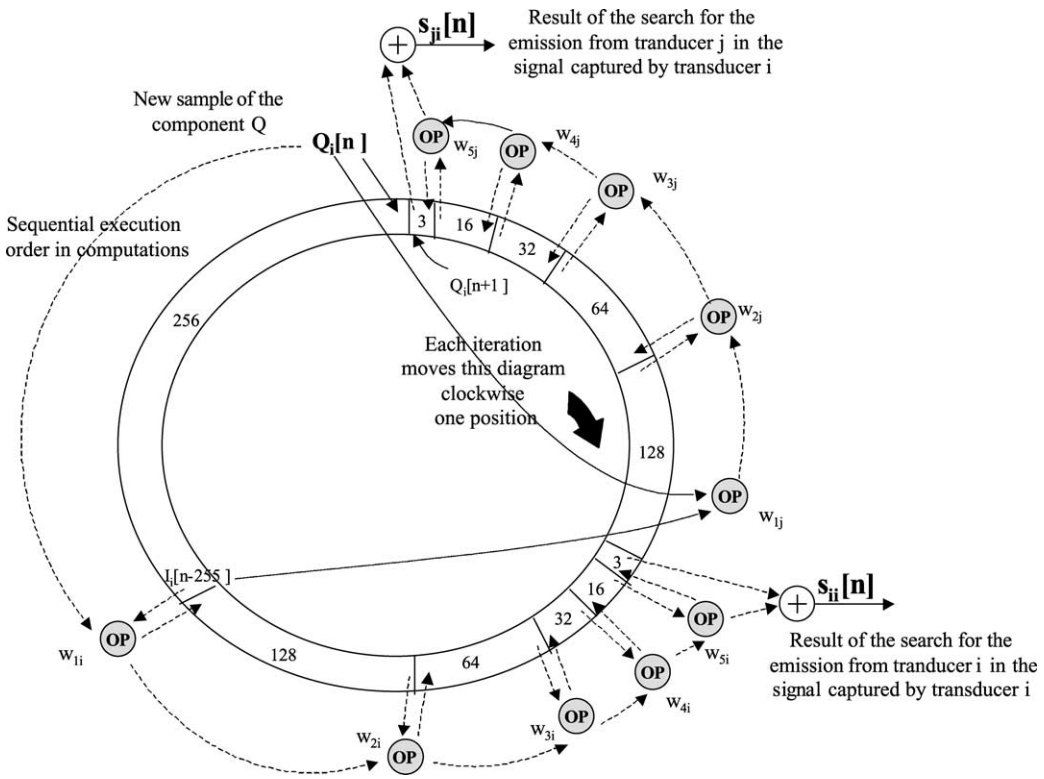

Fig. 11. Diagram of the accesses made to external memory during the execution of the algorithm's second correlation.

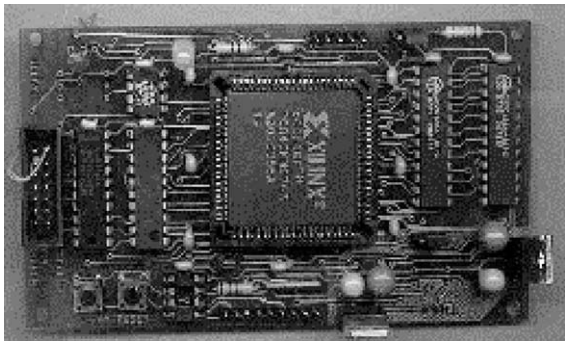

Fig. 12. View of the platform based on a Xilinx XC4000-family FPGA.

the system is 12 MHz to comply with the restrictions of real-time operation.

3. Results

The proposed system has been developed within the framework of an ultrasonic sensor made up of four transducers. Only two of them, those located at the edges, operate as emitters. Each transducer has an associated set of hardware resources on which the algorithm needed to detect the possible echoes from the two emitters is implemented.

These hardware resources are built on a simple platform (see Fig. 12) based on a low-cost FPGA device. This is a 12 MHz Xilinx XC4005 [9] device, to which has been added an external 2 KB memory bank. Using this set-up, several experimental tests have been carried out that have corroborated the validity of the proposed algorithmics.

Fig. 13 shows a real environment, in which two reflectors are located at the front of the sensor, with different inclination angles and distances. Emissions have been made simultaneously from transducers E/R1 and E/R4, in order to confirm that there is no interference between the two emissions. Fig. 14 shows the signal acquired in transducer E/R1 (a) following the simultaneous emission. The system performs the previously described algorithm to this signal in order to detect echoes from the emission made by E/R1 (b) or E/R4 (c). It may be observed how it is possible to identify in these results the echoes produced by both reflectors in the two signals emitted, confirming that there is no crosstalk interference between them. Fig. 15 shows a similar set of data, in this case, for the signal captured by E/R4 (a). As in the earlier case, it is possible to

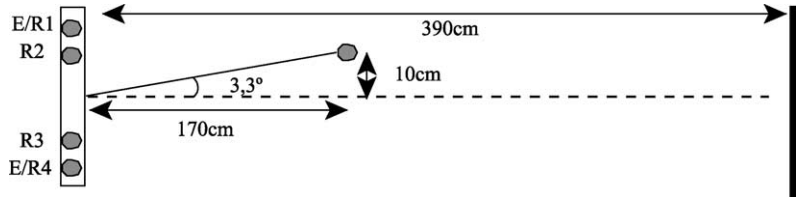

Fig. 13. Example of detection using two reflectors.

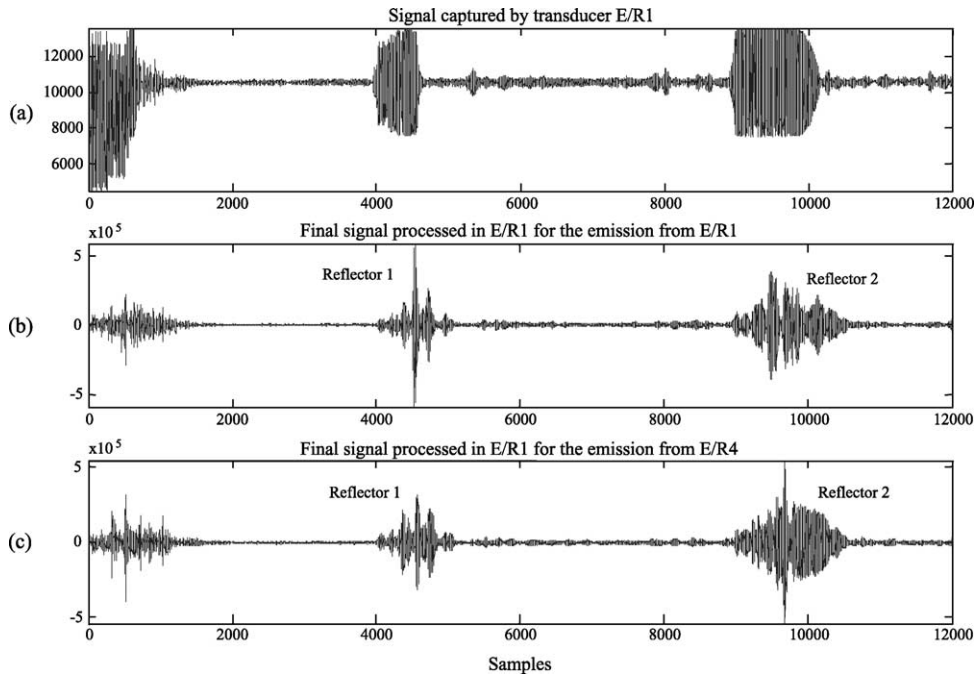

Fig. 14. Detection results in the signal captured by the transducer E/R1.

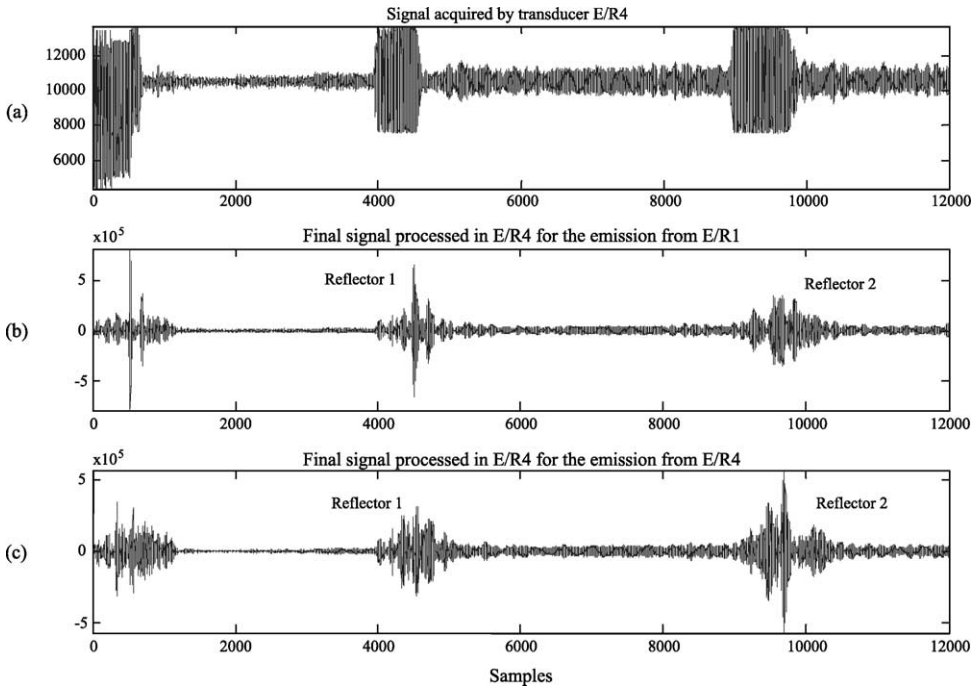

Fig. 15. Detection results in the signal captured by the transducer E/R4.

process this signal in order to detect the echoes from E/R1 (b) and E/R4 (c). Once again, both analyses confirm the existence of echoes from the two emissions.

Taking into account the sensor's geometric distribution, these echoes may be used in high-level algorithms to compute reception angles, classify reflectors, etc. In these tasks, it is necessary to have simultaneous times-of-flight from the same reflector, obtained from different points of emission [4]. This objective has been achieved in this paper.

4. Conclusions

The development of a sensorial system based on ultrasonic transducers attempts to reduce scanning times. A high degree of precision in times-of-flight determination is also desirable in high-level tasks in the robotics field, such as mapping or reflector classification. This paper proposes a system that permits a sensor composed of several transducers to simultaneously perform the emission process from at least two transducers. It allows also to perform the reception process in all transducers. This is made feasible by associating a pair of unequivocal and orthogonal Golay sequences with each emitter, so a receiver is always able to identify the source of the echo that it has received. The use of binary sequences, and the correlation techniques associated with them, implies a notable increase in the precision of the times-of-flight, which may later be used, in conjunction with triangulation and trigonometric techniques, for high-level tasks.

Furthermore, a hardware architecture has been developed that enables satisfactory real results to be obtained and implemented using all of the proposed algorithmics. For this purpose, low-range programmable logic devices have been used, what have enabled one of the main characteristics of the ultrasonic sensorial systems to be maintained, namely their low cost.

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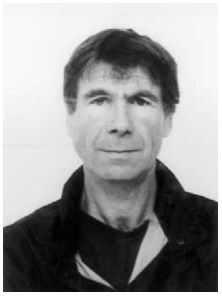

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